DOCUMENT-IDENTIFIER: US 5357621 A
TITLE: Serial architecture for memory module control

ABPL:
An expandable memory system including a central memory controller and one or more plug-in memory modules, each memory module having an on-board memory module controller coupled in a serial network architecture which forms a memory

command link Each memory module controller is serially linked to the central memory controller. The memory system is automatically configured by the central controller, each memory module in the system is assigned a base address, in turn, to define a contiguous memory space without user intervention or the requirement to physically reset switches. The memory system includes the capability to disable and bypass bad memory modules and reassign memory addresses without leaving useable memory unallocated.

BSPR:
The present invention provides an expandable memory system for use in a computing system which comprises a plurality of plug-in memory modules coupled to a memory system controller in a serial network. The memory system network consists of a central memory system controller and at least one individually addressable memory module controller coupled serially to the memory system controller. Various command signals generated by the memory system controller and information or data signals generated either by the memory system controller or individual memory module controllers in response to commands transmitted from the system controller, are transmitted and received serially between the system controller and the memory module controllers . In the preferred embodiment, up to 7 module controllers and their associated memory modules may be configured in the serial network.

BSPR:
The expandable memory system of the present invention utilizes a plurality of plug-in, add-on memory modules or memory cards wherein each individual memory module comprises a module controller, a module memory address control logic block and at least one memory block having a number of individually addressable memory cells. Each memory module also includes a bi-directional 16-bit data bus, an address bus and an address control bus and primary and secondary module connectors respectively attached to opposite sides of the memory module card.

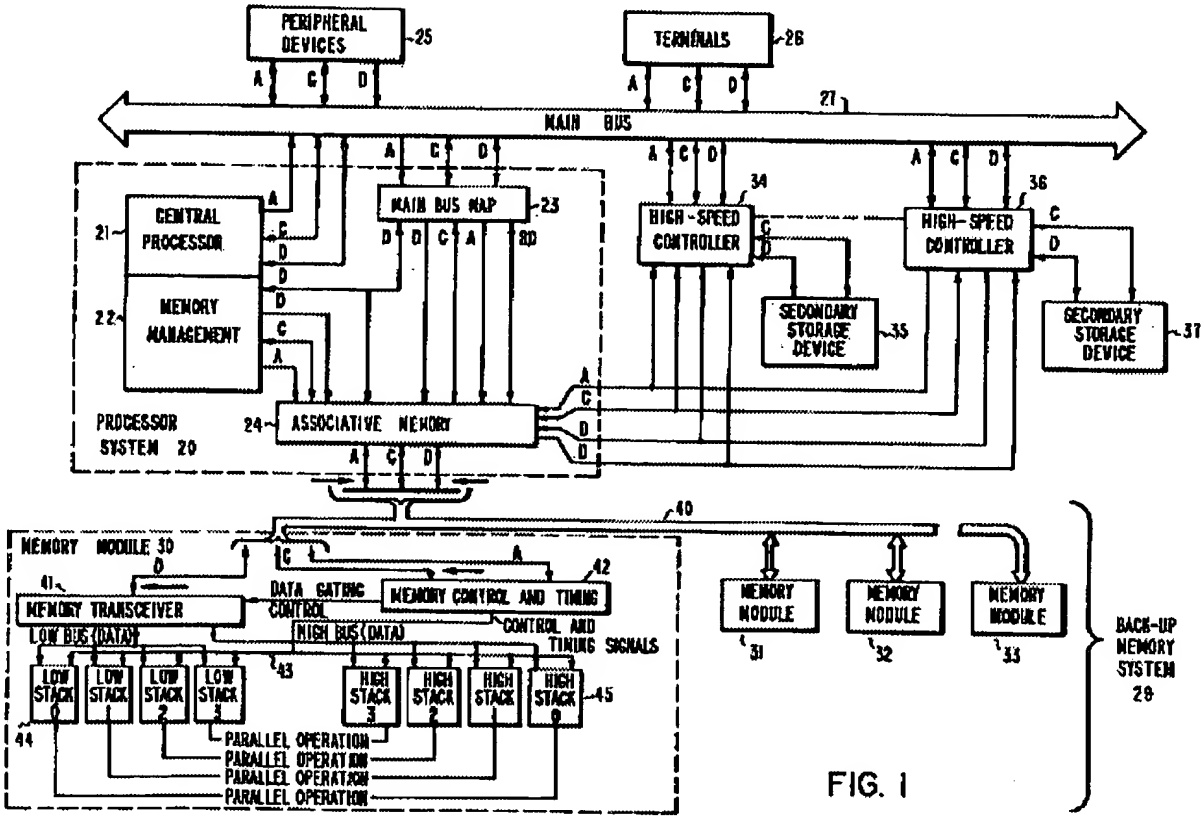
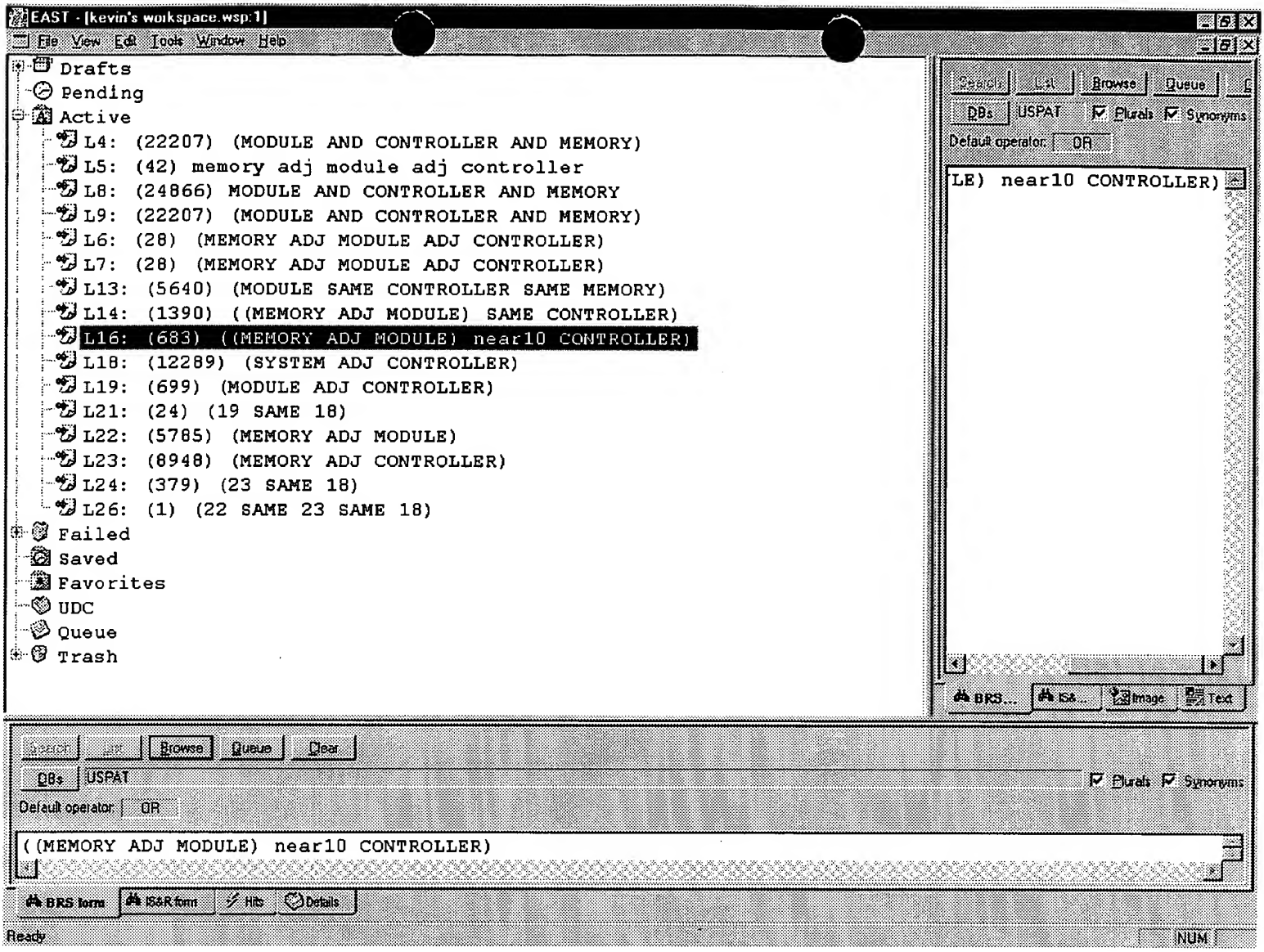


FIG. 1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DERWENT-ACC-NO: 1999-052331
DERWENT-WEEK: 199905

TITLE: Memory module controller for SDRAM - includes voltage control multiphase clock generator that controls voltage level of S receiver as well as
D receiver between which data transmission occurs
PATENT-ASSIGNEE: TOSHIBA KK[TOKE]
PRIORITY-DATA: 1997JP-0109126 (April 25, 1997)
PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10303727 A	November 13, 1998	N/A	015	H03K 019/0175

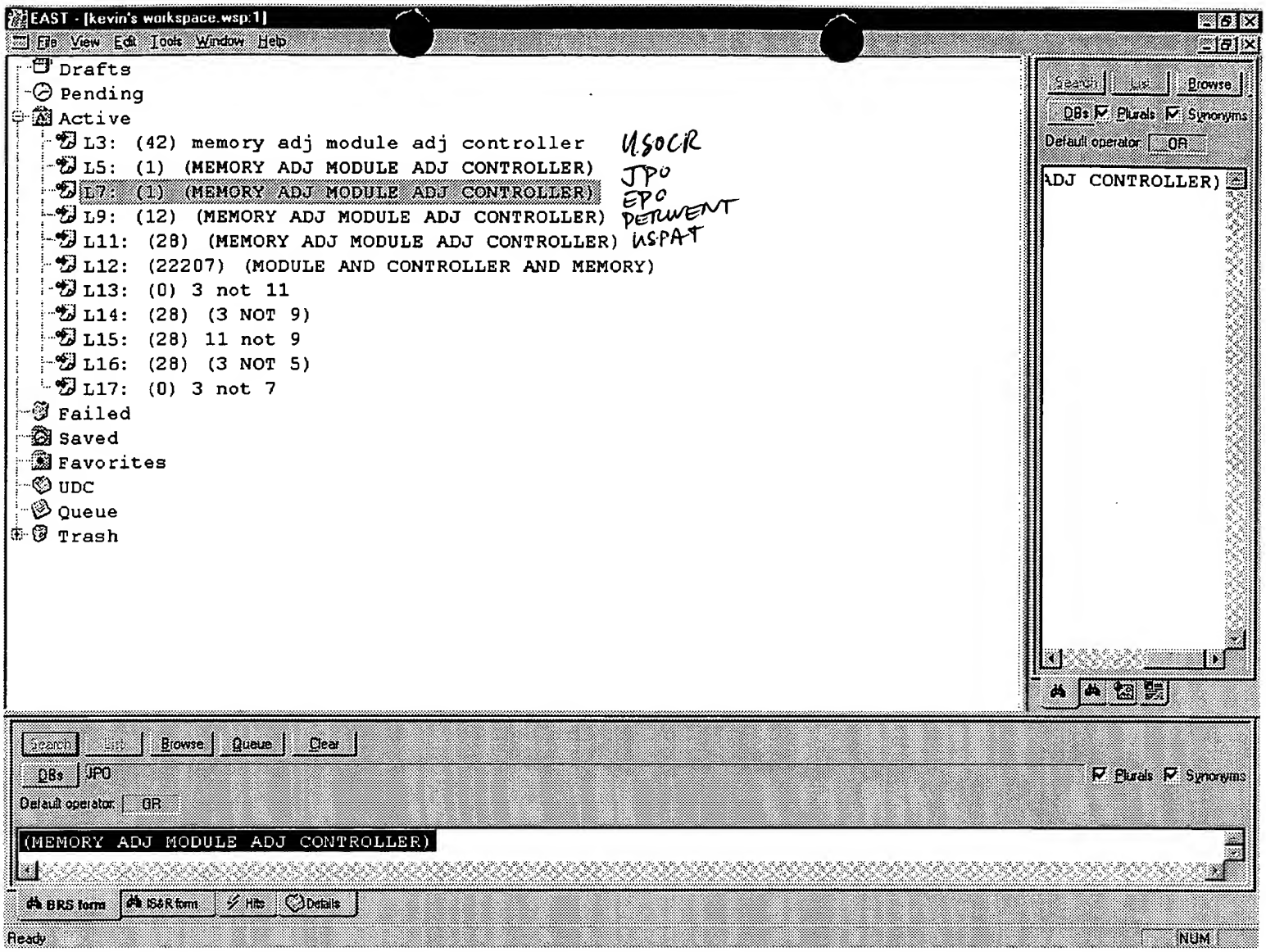
APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP10303727A	N/A	1997JP-0109126	April 25, 1997

INT-CL_(IPC): G11C011/407; H03K003/02 ; H03K019/0175
ABSTRACTED-PUB-NO: JP10303727A
BASIC-ABSTRACT: The controller consists of an S receiver (11) that receives a return clock (QS). Based on the received return clock, a multiphase clock from
a clock generator (13) is transferred at predetermined timings to a D receiver

(12) which transfers received data (DQ).

ADVANTAGE - Generates data fetching time reliably.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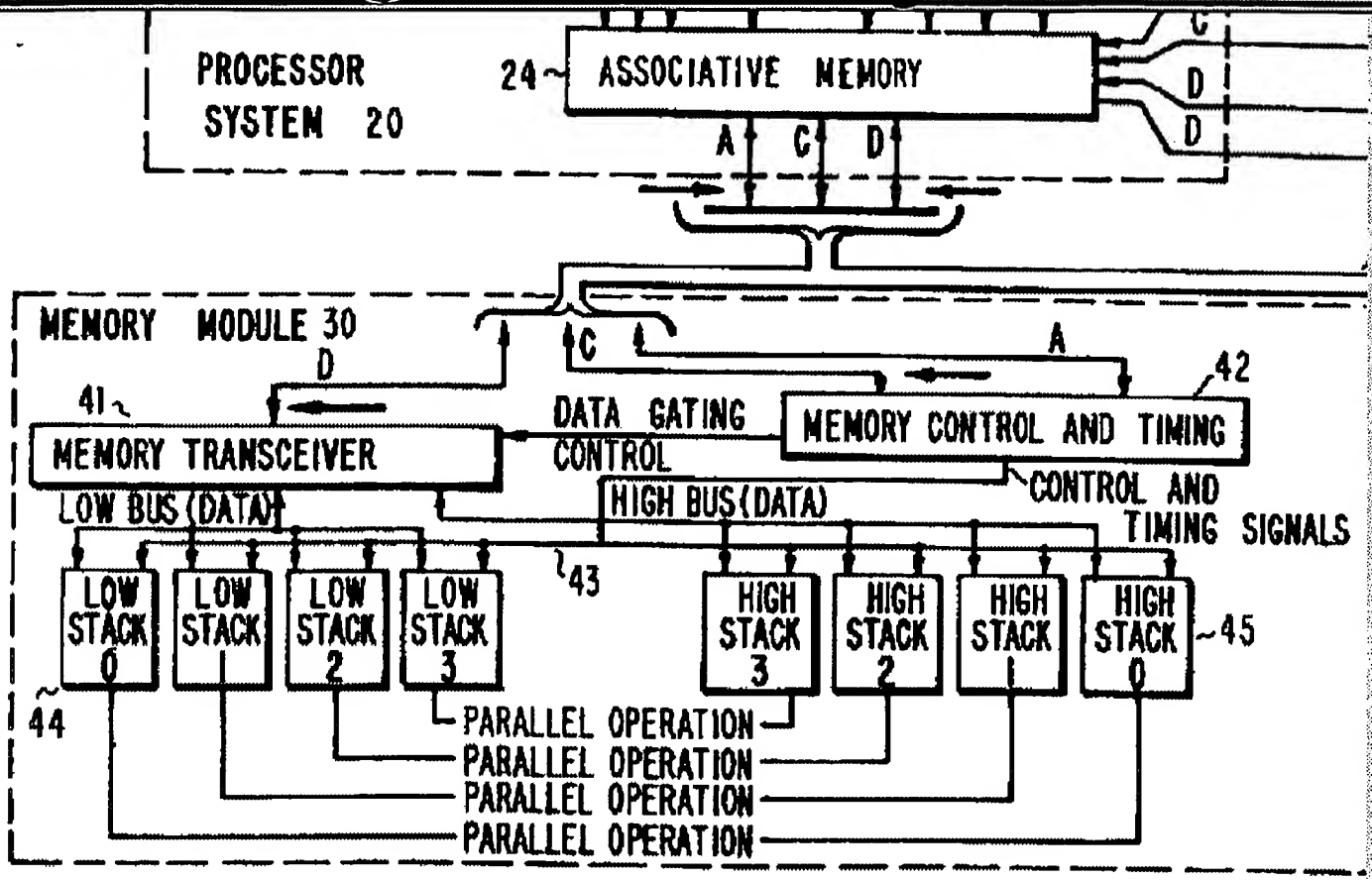

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